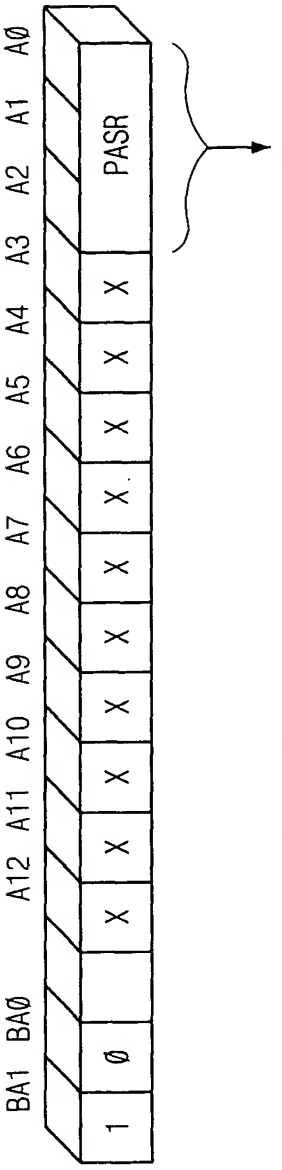

A2	A1	A0	SELF REFRESH TYPE
0	0	0	ALL BANKS
0	0	1	HALF ARRAY (BA1=0)
0	1	0	QUARTER ARRAY (BA1=BA0=0)
0	1	1	RFU
1	0	0	RFU
1	0	1	HALF OF BANK (BA1=BA0=ROW ADDRESS MSB=0)
1	1	0	QUARTER OF BANK (BA1=BA0=ROW ADDRESS2 MSBs=0)
1	1	1	RFU

Fig.1

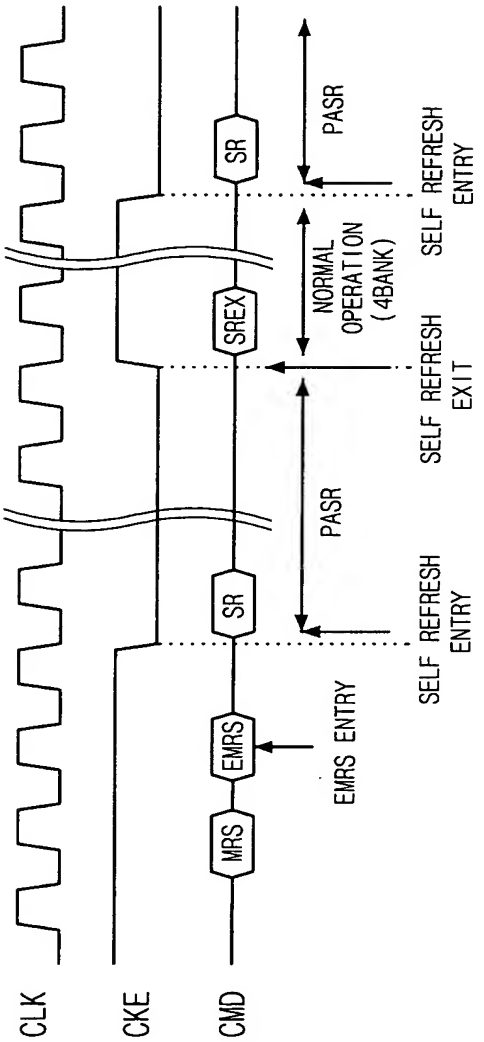
CLK
CKE
CMD
MRS
EMRS
SR
SREX
SR
EMRS ENTRY
SELF REFRESH ENTRY
PASR
SELF REFRESH EXIT
NORMAL OPERATION (4BANK)
SELF REFRESH ENTRY
PASR

Fig.2

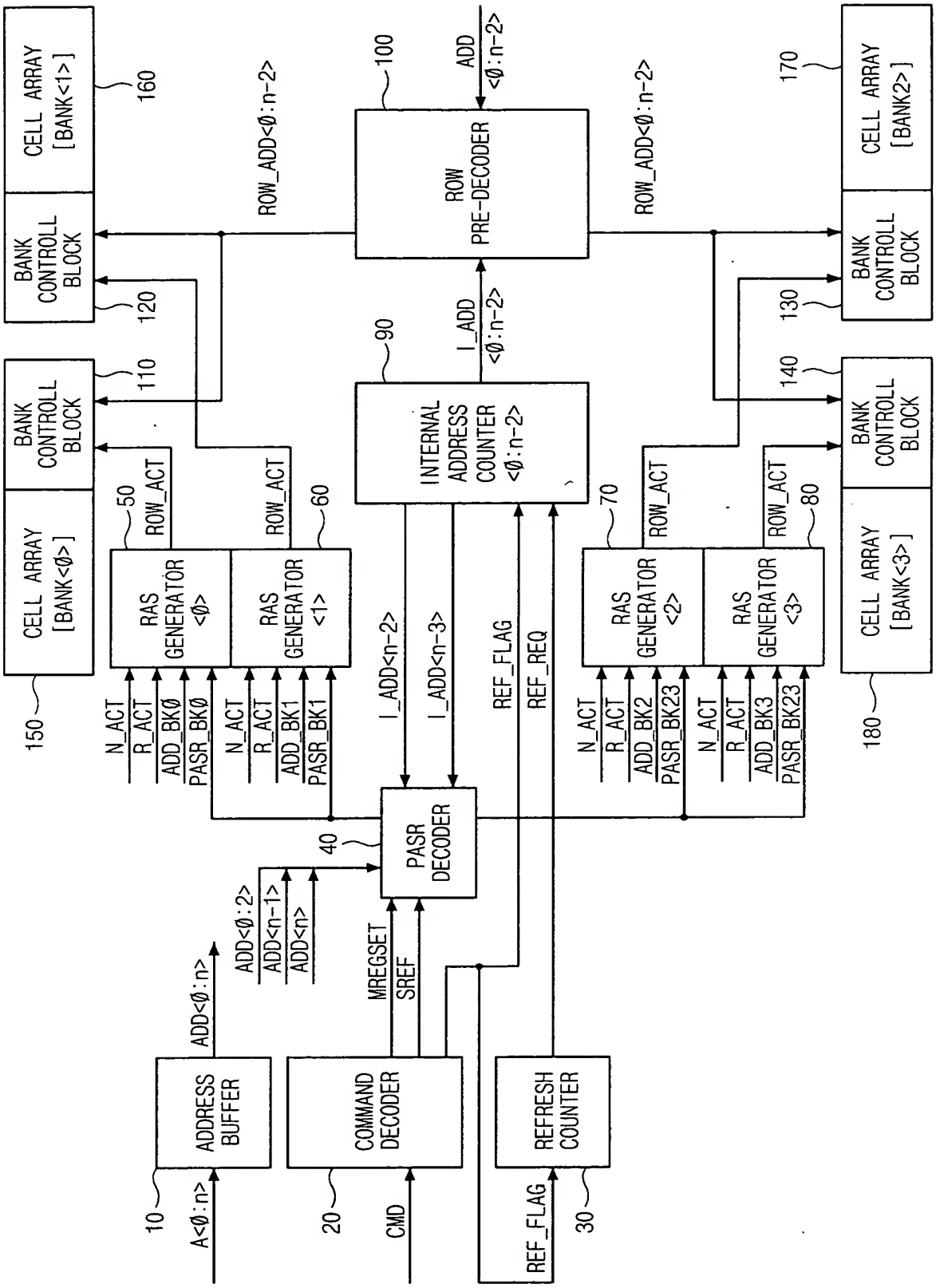
CELL ARRAY [BANK<1>]
160
BANK CONTROLL BLOCK
120
ROW_ADD<Ø:n-2>
100
ROW PRE-DECODER
ADD <Ø:n-2>
170
CELL ARRAY [BANK2>]
BANK CONTROLL BLOCK
130
BANK CONTROLL BLOCK
110
90
I_ADD <Ø:n-2>
140
BANK CONTROLL BLOCK
INTERNAL ADDRESS COUNTER <Ø:n-2>
CELL ARRAY [BANK<Ø>]
50
ROW_ACT
60
ROW_ACT
70
ROW_ACT
80
ROW_ACT
RAS GENERATOR <Ø>
RAS GENERATOR <1>
RAS GENERATOR <2>
RAS GENERATOR <3>
CELL ARRAY [BANK<3>]
150
N_ACT
R_ACT
ADD_BKØ
PASR_BKØ
N_ACT
R_ACT
ADD_BK1
PASR_BK1
I_ADD<n-2>
I_ADD<n-3>
REF_FLAG
REF_REQ
N_ACT
R_ACT
ADD_BK2
PASR_BK23
N_ACT
R_ACT
ADD_BK3
PASR_BK23
180
PASR DECODER
40
ADD<Ø:2>
ADD<n-1>
ADD<n>
MREGSET
SREF
ADD<Ø:n>
ADDRESS BUFFER
COMMAND DECODER
REFRESH COUNTER
10
A<Ø:n>
20
CMD
REF_FLAG
30

Fig.3

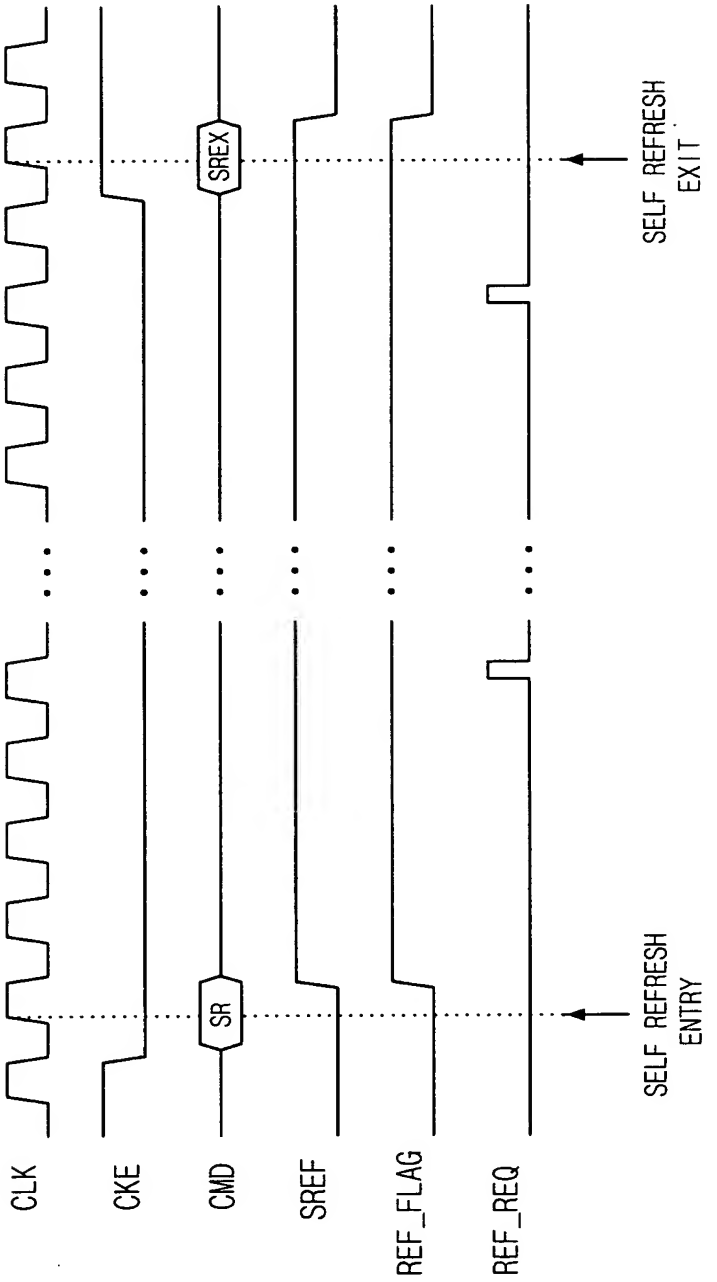
CLK
CKE
CMD
SREF
REF_FLAG
REF_REQ
SR
SREX
SELF REFRESH ENTRY
SELF REFRESH EXIT

Fig.4

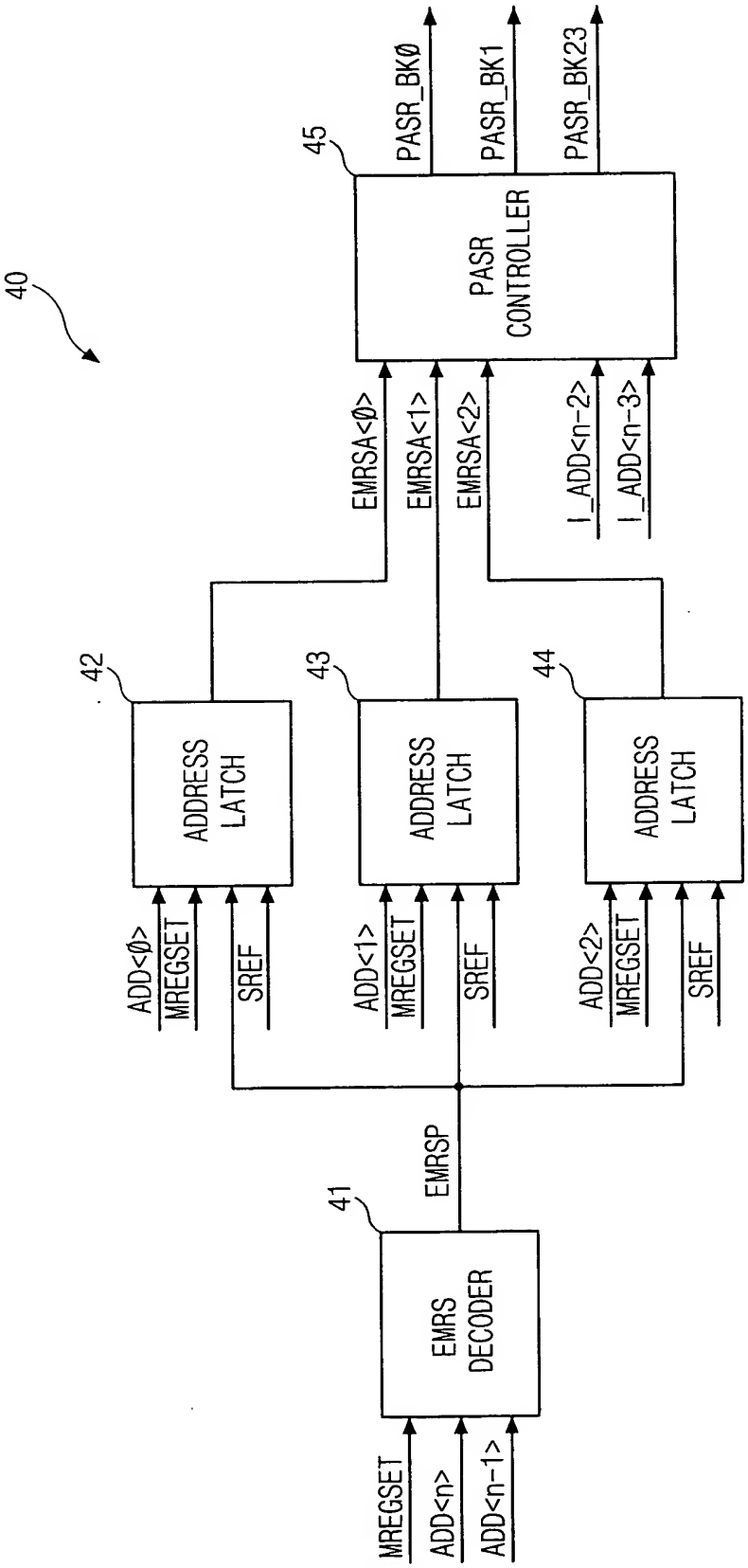
40
45
PASR_BK0
PASR_BK1
PASR_BK23
PASR CONTROLLER
EMRSA<0>
EMRSA<1>
EMRSA<2>
I_ADD<n-2>
I_ADD<n-3>
42
43
44
ADDRESS LATCH
ADDRESS LATCH
ADDRESS LATCH
ADD<0>
MREGSET
SREF
ADD<1>
MREGSET
SREF
ADD<2>
MREGSET
SREF
EMRSP
41
EMRS DECODER
MREGSET
ADD<n>
ADD<n-1>

Fig.5

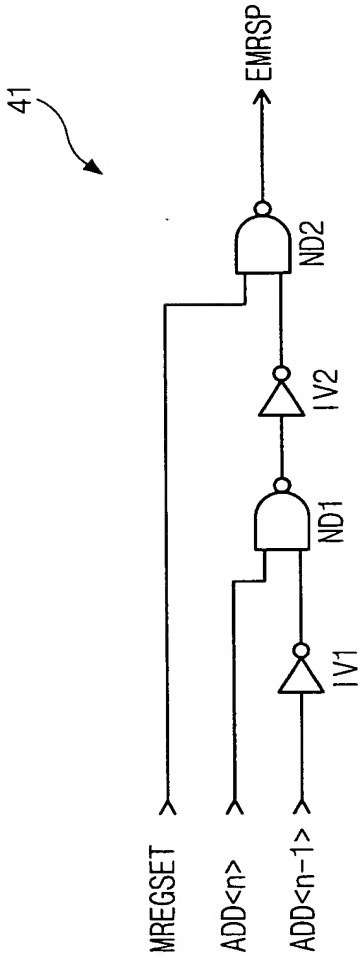

Fig.6

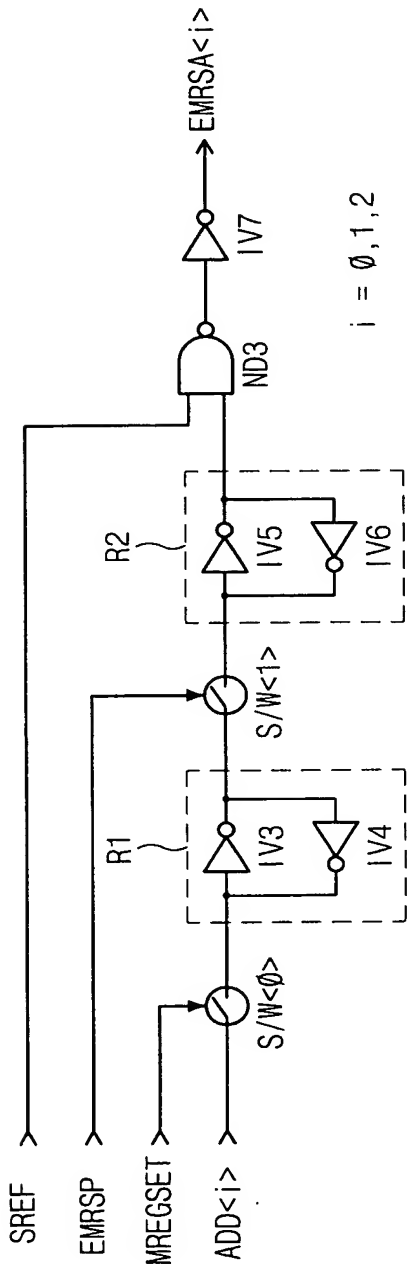
EMRSA<i>
IV7
ND3
i = Ø,1,2
R2
IV5
IV6
S/W<1>
R1
IV3
IV4
S/W<Ø>
SREF
EMRSP
MREGSET
ADD<i>

Fig.7

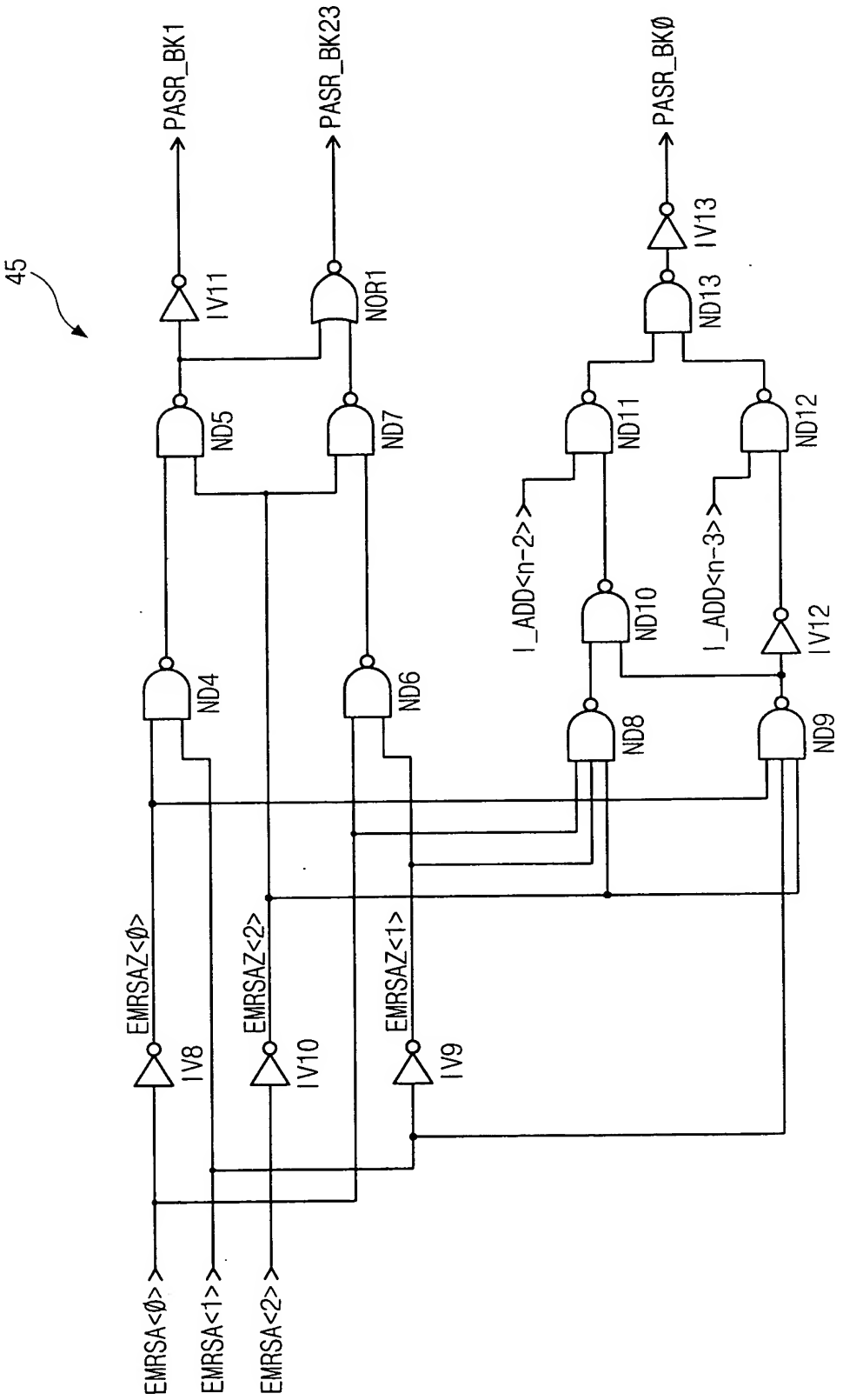
45
PASR_BK1
PASR_BK23
PASR_BKØ
IV11
NOR1
IV13
ND13
ND5
ND7
ND11
ND12
I_ADD<n-2>
I_ADD<n-3>
ND10
IV12
ND4
ND6
ND8
ND9
EMRSAZ<Ø>
EMRSAZ<2>
EMRSAZ<1>
IV8
IV10
IV9
EMRSA<Ø>
EMRSA<1>
EMRSA<2>

Fig.8

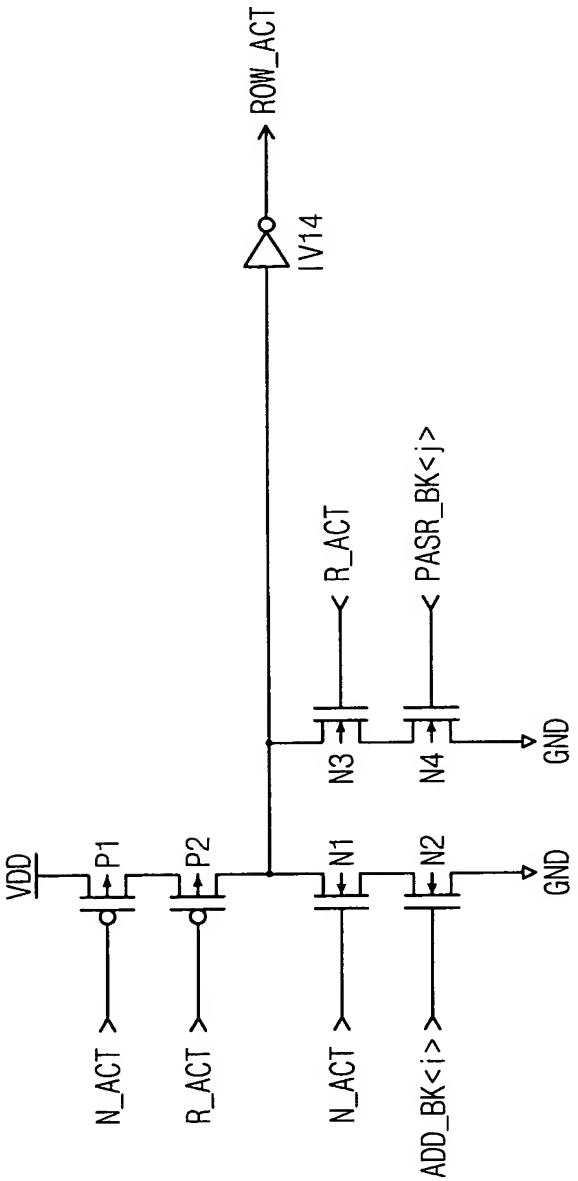
ROW_ACT
IV14
R_ACT
PASR_BK<i>
N3
N4
GND
VDD
P1
P2
N1
N2
GND
N_ACT
R_ACT
N_ACT
ADD_BK<i>

Fig.9

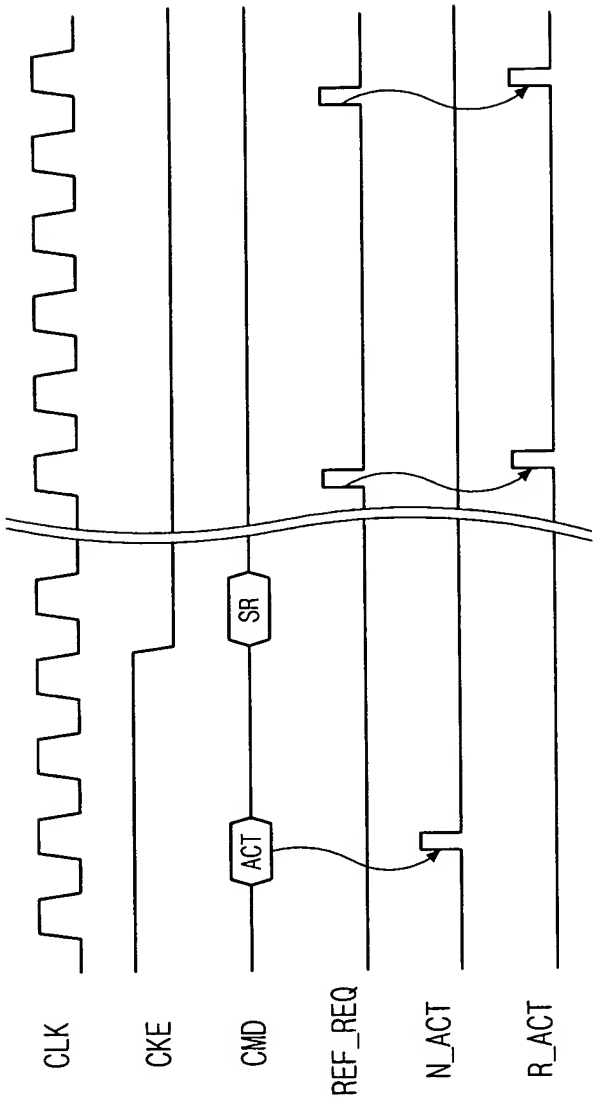

Fig.10